AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 28 and 30 as shown below.

The following is a complete list of all claims in this application.

1-27. (Cancelled)

28. (Currently Amended) A thin film transistor array panel, comprising:

a plurality of pixels defined by gate lines and data lines; and

a plurality of thin film transistors and pixel electrodes formed at the pixel and electrically connected to the gate lines and the data lines,

wherein ~~a semiconductor layers of the~~ thin film transistors have a semiconductor layer and an ohmic layer, said semiconductor layer having a double-layered structure with a lower layer and an upper layer ~~including~~ made of amorphous silicon layers~~,~~ which have different~~,~~ band gaps.

29. (Currently Amended) The thin film transistor array panel of claim 28, wherein the ~~semiconductor layers include a first amorphous silicon layer and a second~~ upper amorphous silicon layer is formed on the ~~first~~ lower amorphous silicon layer, wherein the band gap of the ~~second~~ upper amorphous silicon layer is ~~lower~~ less than that of the ~~first~~ lower amorphous silicon layer.

30. (Currently Amended) A thin film transistor array panel, comprising:

a plurality of pixels defined by gate lines and data lines; and

a plurality of thin film transistors and pixel electrodes formed at the pixel and electrically connected to the gate lines and the data lines,

wherein ~~a~~ thin film transistors have a gate insulating layer ~~that is one element of the thin film transistor~~, said gate insulating layer having a double-layered structure including a lower insulating layer and an upper insulating layer, wherein one of the insulating layers is composed of an organic insulating material, and the other is composed of at least one of amorphous silicon nitride and amorphous silicon oxide.

31-35 (Cancelled)